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Building Flexible SoCs

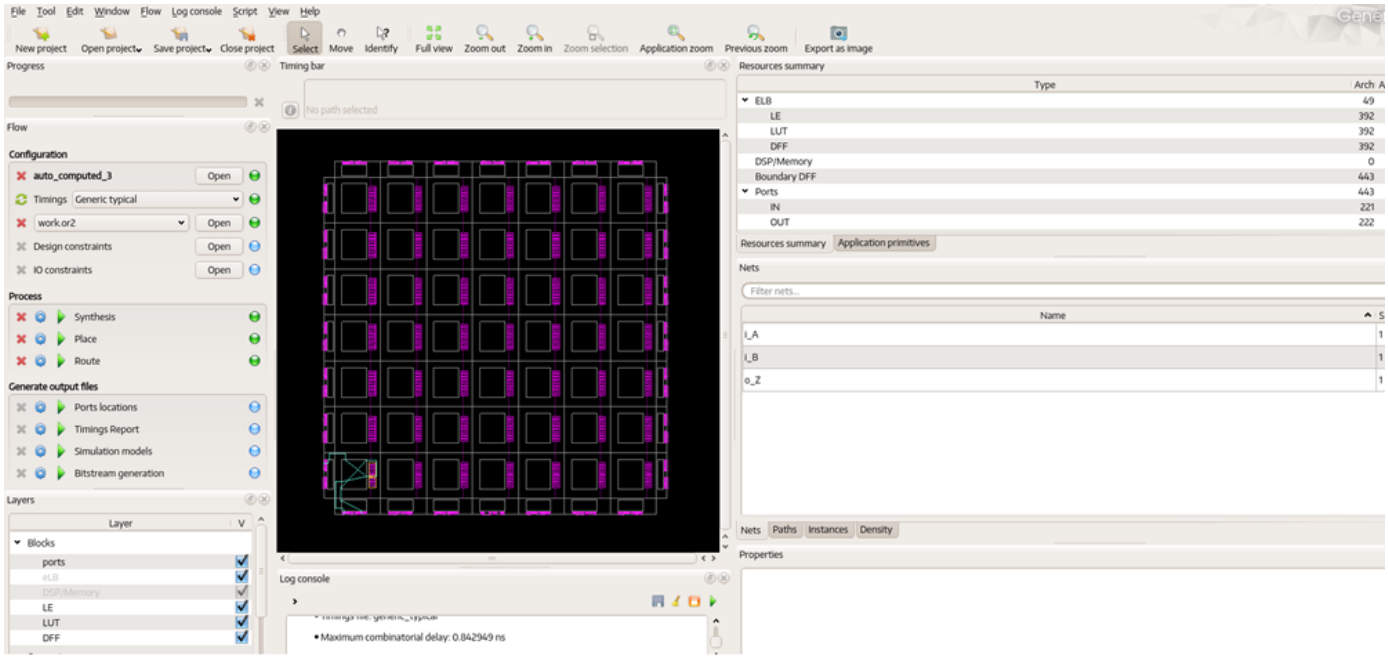
Origami™ Designer & Programmer

Integrated software tool environment for designing with embedded FPGAs

Menta® Origami Designer and Programmer provide an integrated design environment for implementing your design using Menta embedded FPGAs IPs.
***Origami Designer** lets you explore and evaluate different hardware architecture options to meet target specifications.*
***Origami Programmer** synthesizes your RTL and guides you toward generating an optimized bitstream to program the eFPGA that will meet your goals for resource-utilization, clock-speed, latency and throughput.*

Key features and benefits

- Intuitive and easy design and exploration of custom eFPGA architectures
- Synthesis and place-and-route capabilities
- SDC timing-driven flow
- Verific® parser supports design-inputs written in IEEE RTL VHDL/Verilog and System Verilog
- Automated area and power estimation on selected processes and V/T corners
- 100% TCL support enables tool-flow scripting
- Fast RTL simulation model generation with SDF back annotation
- Licensing supports bitstream generation in the field by end customers
- Runs on RedHat Linux 6.x/7.x and SUSE Linux 11/12
- Advanced analysis such as STA or congestion map



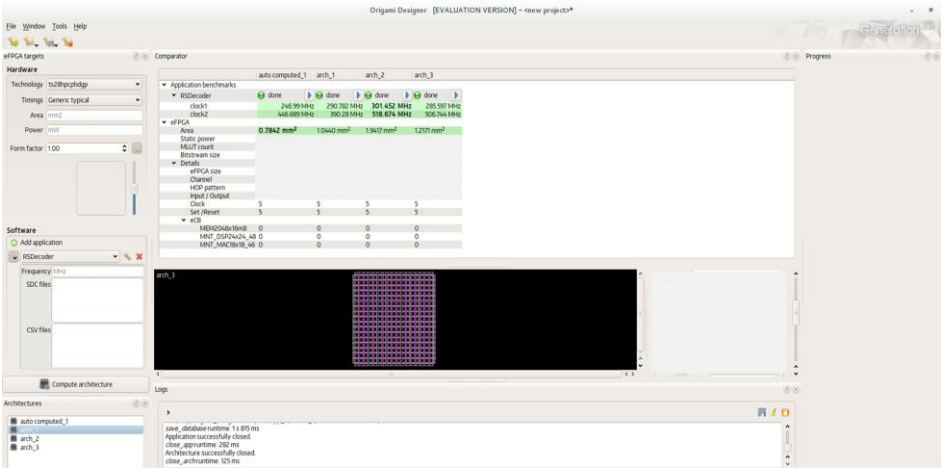
Origami Designer

eFPGA specification software. As a starting-point, Menta offers a complete family of reference eFPGAs ready to be used "out-of-the-box." Using Origami Designer, you can go a step further and create your own customized eFPGA by specifying: number of lookup tables (LUTs), number and configuration of Menta adaptive DSP, RAMs and number/type of interconnects. The output from Origami Designer is then used to generate GDSII for a customized eFPGA delivery from Menta to the customer. Other business model options are available. This enables you to

architect the optimum eFPGA you want to suit your application.

Automatic or manual eFPGA architecture creation. Origami Designer lets you automatically generate different eFPGA architectures by having the tool analyze your RTL code. But if you have very specific requirements, you can also manually input specific hardware parameters, such as size and form factor

Graphical exploration and analysis. After generating the set of candidate architectures you want, Origami Designer provides a "dashboard" showing specifications for each of those different architectures, enabling you to thoroughly compare them side by side in order to make the optimal size vs. performance trade-offs for your targeted application. Finally, once you have selected the eFPGA architecture you want to use, you can save it within a Menta Architecture File (MAF), which is then used by the Menta IP delivery team to generate a customized eFPGA hard IP. The MAF file can also serve as an input to Origami Programmer.



Origami Programmer

Best-in-class eFPGA programming software. Origami Programmer provides all the capabilities designers expect from today's best-in-class FPGA design environments. Origami Programmer's synthesis, mapping, place-and-route capabilities, together with its fast runtime and intuitive graphical interface, enable designers to rapidly evaluate and generate the optimum bitstream for programming their eFPGA, with quality of results (QoR) comparable to leading commercial FPGA vendors.

Simulation and verification in your EDA flow. Besides outputting performance estimations for analysis, Origami Programmer also generates fast/abstracted simulation models that can be used in any simulation/verification flow, and for functional equivalence checking. The generated models are compatible with all major EDA flows.

GUI and TCL interfaces. Origami Programmer also supports full programmability of the design flow using Tool Command Language (TCL). At each stage of the flow, designers have access to easy-to-use analysis tools through the GUI, such as STA analysis or congestion maps.

Timing and IO constraints. Origami Programmer supports a subset of the SDC format for timing driven place & route. IO placement constraints are supported through a simple CSV file.

Advanced features. Origami Programmer offers graphical floorplanning capability, multiple synthesis and routing options to optimize for resources utilization or speed, and automatic inferring of memory and DSP blocks.

High Level Synthesis. Origami Programmer supports High Level Synthesis (HLS) capability to program the eFPGA IP in SystemC or C++ in concert with Mentor Graphics Catapult™.

Fast learning curve. It takes less than half a day for an experienced FPGA designer to master both Origami Designer and Origami Programmer.

Datasheets, Menta Starter Pack training & evaluation software on any process node, as well as TSMC 28HPC+ evaluation board are available. For more information visit our website at: www.menta-efpga.com

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